**EAST WEST UNIVERSITY**

**Semester:** Fall 2016

**Course Number:** CSE 345

**Course Title:** Digital Logic Design

**Experiment No:** 03

**Experiment Title:** Behavioral Verilog Simulation of a Combinational Logic Circuit

**Name:** Md. Sakibur Rahman

**ID:** 2014-1-60-032

**Group Number:** 02

**Group IDs:**

2014-1-60-032

2014-1-60-

2014-1-60-

2014-1-60-0

**Date of Performance:** October 19, 2016

**Objectives:**

1. To learn behavioral Verilog coding of a combinational logic circuits using procedural model.

2. To learn behavioral Verilog coding of a combinational logic circuits using continuous assign statement.

**Answers to the Pre-Lab Questions**

1. **S= A'B'C+ A'BC'+ AB'C'+ ABC**

**Procedural Code:**

module expt(output S,

input A,B,C);

always @(A,B,C)

begin

S=0;

if (~A&~B&C)

S=1;

if (~A&B&~C)

S=1;

if (A&~B&~C)

S=1;

if (A&B&C)

S=1;

end

endmodule

2.

**Continuous Assign Statement:**

S= A'B'C+ A'BC'+ AB'C'+ ABC

module expt (output reg S,

input A,B,C);

assign S=(~A &~B & C) | (~A & B & ~C)| (A & ~B & ~C) | (A & B & C);

endmodule